WHAT IS CLAIMED IS:

1. A system for implementing an electronic architecture, comprising:

a primary device that is configured to perform core operating functions in said electronic architecture;

an auxiliary device that is configured to perform selected additional operating functions in said electronic architecture;

a primary channel configured for performing communications procedures between said primary device and said auxiliary device; and

an auxiliary channel configured for performing data transfer operations between said primary device and said auxiliary device, said communications procedures over said primary channel and said data transfer operations over said auxiliary channel being able to occur in a concurrent manner.

2. The system of claim 1 wherein at least one of said primary device and said auxiliary device is implemented as an integrated circuit device.

3. The system of claim 1 wherein at least one of said primary device and said auxiliary device is implemented to include input/output interface functionalities for an electronic system.

4. The system of claim 1 wherein said core operating functions include predetermined functionalities that remain substantially unchanged over several generations of said electronic architecture.

5. The system of claim 1 wherein said selected additional operating functions include predetermined functionalities that have a potential to change over several generations of said electronic architecture.

6. The system of claim 1 wherein said electronic architecture includes a processor, said primary device, one or more primary peripheral devices, a memory, said auxiliary device, and one or more auxiliary peripheral devices, wherein said CPU, said memory, and said one or more primary peripheral devices each communicate through said primary device, and wherein said one or more auxiliary peripheral devices each communicate through said auxiliary device.

7. The system of claim 1 wherein said primary device includes a CPU interface, one or more peripheral interfaces, a memory interface, a primary channel interface, an auxiliary channel interface, an arbiter, a DMA engine, and an internal primary device bus structure.

8. The system of claim 1 wherein an arbiter performs a primary channel arbitration procedure between a processor and one or more primary peripheral devices for controlling access to said primary channel, said primary channel having electrical connectors coupled to pins of said primary device and to pins of said auxiliary device, said electrical connectors being multiplexed to conserve said pins of said primary device and said pins of said auxiliary device.

9. The system of claim 1 wherein said data transfer operations between said primary device and said auxiliary device over said auxiliary channel are initiated by a processor coupled to said primary device, and then are performed by a direct memory access engine coupled to said primary device.

10. The system of claim 1 wherein said auxiliary device includes a primary channel interface, an auxiliary channel interface, one or more auxiliary configuration registers, one or more auxiliary peripheral interfaces, and an internal auxiliary device bus structure.

11. The system of claim 1 wherein a processor coupled to said electronic architecture determines whether an auxiliary configuration procedure is required to configure said auxiliary device in response to at least one of a powerup event and a dynamic operational event.

12. The system of claim 11 wherein an arbiter coupled to said primary device performs an arbitration procedure for several entities in said electronic architecture to thereby grant control of said primary channel to said processor.

13. The system of claim 11 wherein said processor programs auxiliary configuration registers coupled to said auxiliary device to setup said auxiliary device for performing one or more corresponding auxiliary procedures.

14. The system of claim 1 wherein a processor coupled to said electronic architecture determines whether one of said communications procedures is required between said primary device and said auxiliary device.

15. The system of claim 14 wherein an arbiter coupled to said primary device performs an arbitration procedure for several entities in said electronic architecture to thereby grant control of said primary channel to said processor.

16. The system of claim 14 wherein said processor communicates with said auxiliary device through said primary device during said one of said communications procedures.

17. The system of claim 1 wherein a processor coupled to said electronic architecture determines whether one of said data transfer operations is required between a memory device and said auxiliary device, said processor responsively setting up a direct memory access engine that is coupled to said primary device.

18. The system of claim 17 wherein said processor instructs said direct memory access engine to initiate said one of said data transfer operations between said memory device and said auxiliary device through said primary device, said direct memory access engine responsively beginning and then controlling said one of said data transfer operations.

19. The system of claim 18 wherein said direct memory access engine determines that said data transfer operation is complete, said direct memory access engine responsively notifying said processor.

20. The system of claim 1 wherein an auxiliary direct memory access engine coupled to said auxiliary device determines that one of said data transfer operations is required between a memory device and said auxiliary device, said auxiliary direct memory access engine responsively setting up and controlling said one of said data transfer operations.

21. A method for implementing an electronic architecture, comprising the steps of:

performing core operating functions in said electronic architecture by utilizing a primary device;

performing selected additional operating functions in said electronic architecture by utilizing an auxiliary device;

performing communications procedures between said primary device and said auxiliary device by utilizing a primary channel; and

performing data transfer operations between said primary device and said auxiliary device by utilizing an auxiliary channel, said communications procedures over said primary channel and said data transfer operations over said auxiliary channel being able to occur in a concurrent manner.

22. The method of claim 21 wherein at least one of said primary device and said auxiliary device is implemented as an integrated circuit device.

23. The method of claim 21 wherein at least one of said primary device and said auxiliary device is implemented to include input/output interface functionalities for an electronic system.

24. The method of claim 21 wherein said core operating functions include predetermined functionalities that remain substantially unchanged over several generations of said electronic architecture.

25. The method of claim 21 wherein said selected additional operating functions include predetermined functionalities that have a potential to change over several generations of said electronic architecture.

26. The method of claim 21 wherein said electronic architecture includes a processor, said primary device, one or more primary peripheral devices, a memory, said auxiliary device, and one or more auxiliary peripheral devices, wherein said CPU, said memory, and said one or more primary peripheral devices each communicate through said primary device, and wherein said one or more auxiliary peripheral devices each communicate through said auxiliary device.

27. The method of claim 21 wherein said primary device includes a CPU interface, one or more peripheral interfaces, a memory interface, a primary channel interface, an auxiliary channel interface, an arbiter, a DMA engine, and an internal primary device bus structure.

28. The method of claim 21 wherein an arbiter performs a primary channel arbitration procedure between a processor and one or more primary peripheral devices for controlling access to said primary channel, said primary channel having electrical connectors coupled to pins of said primary device and to pins of said auxiliary device, said electrical connectors being multiplexed to conserve said pins of said primary device and said pins of said auxiliary device.

29. The method of claim 21 wherein said data transfer operations between said primary device and said auxiliary device over said auxiliary channel are initiated by a processor coupled to said primary device, and then are performed by a direct memory access engine coupled to said primary device.

30. The method of claim 21 wherein said auxiliary device includes a primary channel interface, an auxiliary channel interface, one or more auxiliary configuration registers, one or more auxiliary peripheral interfaces, and an internal auxiliary device bus structure.

31. The method of claim 21 wherein a processor coupled to said electronic architecture determines whether an auxiliary configuration procedure is required to configure said auxiliary device in response to at least one of a powerup event and a dynamic operational event.

32. The method of claim 31 wherein an arbiter coupled to said primary device performs an arbitration procedure for several entities in said electronic architecture to thereby grant control of said primary channel to said processor.

33. The method of claim 31 wherein said processor programs auxiliary configuration registers coupled to said auxiliary device to setup said auxiliary device for performing one or more corresponding auxiliary procedures.

34. The method of claim 21 wherein a processor coupled to said electronic architecture determines whether one of said communications procedures is required between said primary device and said auxiliary device.

35. The method of claim 34 wherein an arbiter coupled to said primary device performs an arbitration procedure for several entities in said electronic architecture to thereby grant control of said primary channel to said processor.

36. The method of claim 34 wherein said processor communicates with said auxiliary device through said primary device during said one of said communications procedures.

37. The method of claim 21 wherein a processor coupled to said electronic architecture determines whether one of said data transfer operations is required between a memory device and said auxiliary device, said processor responsively setting up a direct memory access engine that is coupled to said primary device.

38. The method of claim 37 wherein said processor instructs said direct memory access engine to initiate said one of said data transfer operations between said memory device and said auxiliary device through said primary device, said direct memory access engine responsively beginning and then controlling said one of said data transfer operations.

39. The method of claim 38 wherein said direct memory access engine determines that said data transfer operation is complete, said direct memory access engine responsively notifying said processor.

40. The method of claim 21 wherein an auxiliary direct memory access engine coupled to said auxiliary device determines that one of said data transfer operations is required between a memory device and said auxiliary device, said auxiliary direct memory access engine responsively setting up and controlling said one of said data transfer operations.

41. The method of claim 21 wherein communications procedures and said data transfer operations are initiated by a central processing unit in response to one of a notification event from said auxiliary device and a polling event from said central processing unit to said auxiliary device.

42. A system for implementing an electronic architecture, comprising:

means for performing core operating functions in said electronic architecture;

means for performing selected additional operating functions in said electronic architecture;

means for performing communications procedures between said primary device and said auxiliary device; and

means for performing data transfer operations between said primary device and said auxiliary device, said communications procedures and said data transfer operations being able to occur in a concurrent manner.

43. A system for implementing an electronic architecture, comprising:

a primary device that is configured to perform core operating functions in said electronic architecture;

an auxiliary device that is configured to perform selected additional operating functions in said electronic architecture;

a primary channel configured for performing communications procedures between said primary device and said auxiliary device; and

an auxiliary channel configured for performing data transfer operations between said primary device and said auxiliary device.